AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at line 16 of page 7 and ending at line 24 of page 7 with the following amended paragraph:

The data register (buffer memory) 4 is made of, for example, SRAMs or the like. The data register 4 has a depth of N bits (e.g., 10 bits) and disposed as an array of each pixel. The number of arrays of the data register 4 is equal to the horizontal pixel number (m) of the light receiving area 2. The non-volatile memory area 6 has N x m bits per one pixel row in correspondence with the data register 4. Namely, analog signals of one pixel row in the light receiving area 2 ~~6~~ are processed (A/D converted) for respective pixels to obtain parallel digital data of N x m bits which are stored in parallel via the data register 4 into the memory cells corresponding to one row in the non-volatile area 6.